(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 March 2004 (04.03.2004)

PCT

(10) International Publication Number
WO 2004/019123 A1

(51) International Patent Classification[7]: G02F 1/1362, H01L 27/00

(21) International Application Number: PCT/IB2003/003484

(22) International Filing Date: 6 August 2003 (06.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0219771.3 24 August 2002 (24.08.2002) GB

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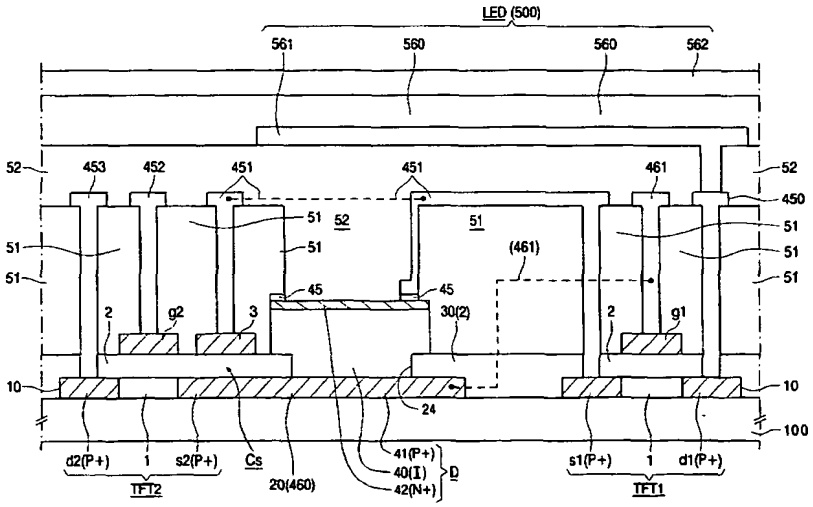
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MANUFACTURE OF ELECTRONIC DEVICES COMPRISING THIN-FILM CIRCUIT ELEMENTS



(57) Abstract: In the manufacture of an electronic device such as an active matrix display, a vertical amorphous PIN photodiode or similar thin-film diode (D) is advantageously integrated with a polysilicon TFT (TFT1, TFT2) in a manner that permits a good degree of optimisation of the respective TFT and diode properties while being compatible with the complex pixel context of the display. High temperature processes for making the active semiconductor film (10) of the TFT more crystalline than an active semiconductor film (40) of the diode and for forming the source and drain doped regions (s1,s2, d1,d2) of the TFT are carried out before depositing the active semiconductor film (40) of the diode. Thereafter. the lateral extent of the diode is defined by etching while protecting with an etch-stop film (30) an interconnection film (20) that can provide a doped bottom electrode region (41) of the diode as well as one of the doped regions (s2, g1) of the TFT.

WO 2004/019123 A1

DESCRIPTION

MANUFACTURE OF ELECTRONIC DEVICES COMPRISING THIN-FILM CIRCUIT ELEMENTS.

This invention relates to methods of manufacturing an electronic device, for example an active matrix display, comprising thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor, the transistor having a channel area in an active semiconductor film that is more crystalline than an active semiconductor film of the diode, for example an amorphous PIN photodiode. The invention also relates to such device structures themselves.

Examples of such devices in the form of active matrix electroluminescent displays are disclosed in published PCT patent applications WO-A-01/20591, WO-A-01/99190 and WO-A-01/99191, the whole contents of which are hereby incorporated herein as reference material. In these electroluminescent display devices, each pixel comprises:

- a light-emitting element, typically a light-emitting diode (LED) of organic semiconductor (for example, polymer semiconductor),
- at least two thin-film transistors (TFTs) of polycrystalline silicon (polysilicon), whereby the LED is driven via a first, drive TFT as addressed via the second, address TFT,
- a thin-film storage capacitor for storing the drive signal applied to the gate of the drive TFT via the address TFT, and
- a light-sensing element (for example, an amorphous PIN photodiode, or a photo-responsive polysilicon TFT) that is responsive to the LED output to provide optical feed-back for regulating LED operation via the drive TFT (in order to counteract aging effects in the LED).

The present invention can be applied to, for example, the integration of the drive and/or address TFT with an amorphous PIN photodiode as the light-sensing element.

As illustrated in WO-A-01/20591, WO-A-01/99190, and WO-A-01/99191, the light-sensing element is connected:

- in parallel with the capacitor, between the gate of the drive TFT and its power supply line (source connection of the drive TFT), and
- between the drive signal output (drain electrode) of the address TFT) and the power supply line (source connection of drive TFT).

In fabricating these display devices, it is generally convenient to form the light-sensing element using common technology and process steps with the TFTs. For this reason, it has been preferable to form the light-sensing element as a photo-sensitive TFT structure (having its gate of ITO or other transparent electrode material connected to its source), or possibly as a lateral PIN diode. In each case, the light-absorbing active semiconductor film of this photo-sensitive TFT structure or PIN diode is provided using the same technology and process steps as the drive and address TFTs of the pixel.

A disadvantage of this approach is that the active semiconductor film (that provides the channel area of the TFTs) is comparatively thin (for example, with a thickness in the range of 0.04μm to 0.10μm). An intrinsic silicon film of this thickness is not fully absorbing at the red end of the spectrum. As a result, different sized photoTFTs/diodes are required for red, green and blue pixels, and the photoTFT/diode for the red is particularly large, consuming useful aperture area. This problem is avoidable if vertical amorphous PIN diodes with thicker silicon are used as the light-sensing elements, but problems then arise as to how best to integrate such vertical diodes with the TFTs in a manner compatible with the display pixel layout.

Similar problems arise with other types of display, for example with the integration of photodiodes in pixels of an active matrix liquid-crystal display (AMLCD). The whole contents of United States patent US-A-5,838,308 are herby incorporated herein as reference material for an example of a need to integrate light-sensing elements in the pixels of an AMLCD for an optical input to the device.

It is an aim of the present invention to facilitate the integration of a thin-film diode (for example a vertical amorphous PIN photodiode) with a more crystalline thin-film transistor in a manner that permits a degree of optimisation of the respective diode and transistor properties, while using common process steps for their integration and while being compatible with even the complex pixel context of an active matrix display.

According to one aspect of the present invention, there is provided a method for the manufacture of such a device, that includes:

(a) forming on a circuit substrate the crystalline active semiconductor film for a channel area of the TFT, with a first process involving a first processing temperature;

(b) forming doped source and drain regions of the TFT at ends of the channel area with a second process involving a second processing temperature;

(c) providing an interconnection film between an electrode area of the TFT and a diode area over which the diode is to be formed, and providing an etch-stop film on which the active semiconductor film for the diode is to be deposited;

(d) thereafter depositing the active semiconductor film for the diode over the interconnection film and the etch-stop film with a third process that involves a third processing temperature, this stage (d) being performed after stages (a) and (b), and the first and second processing temperatures being higher than the third processing temperature; and

(e) thereafter etching away the active semiconductor film for the diode from over the etch-stop to leave the active semiconductor film for the diode over the interconnection film in the diode area.

By carrying out stages (a) and (b) before stage (d), such a method in accordance with the invention is advantageous for the TFT in permitting the achievement of good quality crystalline material for its channel area and of efficient source and drain regions, through the use of the higher first and second processing temperatures. Thus, for example, good polysilicon TFTs can be formed using laser crystallisation of the silicon film and laser annealing of source and drain dopant implants. The source and drain regions can be formed so as to

be self-aligned with the gate electrode of the TFT. Although stages (a) and (b) may be used to provide a bottom-gate TFT, the invention is particularly useful with top-gate TFTs. The TFT may be advantageously hydrogenated after stages (a) and (b) and before the lower temperature stage (d).

By carrying out stage (d) with its lower processing temperature after the higher temperature stages, such a method in accordance with the invention is advantageous for providing the diode with a less crystalline material (for example, even an amorphous semiconductor material) in an appropriate thickness for the desired diode characteristics. Thus, for example, efficient photodiodes of a vertical PIN structure can be formed with an intrinsic hydogenated amorphous silicon (aSi:H) film that is thicker than the polysilicon film of the TFT. Furthermore, de-hydrogenation of this diode film (which would occur if the higher temperature process stages (a) and (b) were carried out subsequently) is avoided by performing these higher temperature process stages (a) and (b) before providing the aSi:H film of the diode. The resulting diode may advantageously exploit a hybrid of amorphous and polysilicon technologies

Furthermore, by depositing and etching the active semiconductor film for the diode over the etch-stop film (as well as over the interconnection film), the layout of this semiconductor film in the diode area can be defined without undesirable etching of other parts of the device such as the TFT and its interconnection to the diode. Such a method in accordance with the invention permits the use of some common films for the TFT and the diode. Thus, for example, the interconnection film can form gate or source/drain connections to the TFT and/or a bottom connection to the diode, whereas another film may provide a top connection to the diode in, for example, a display pixel layout. The interconnection film may even provide the gate electrode or source and drain regions of the TFT and/or an electrode region of the diode. In this manner, the height of stepped increases in the topography due to the integration of a thick vertical diode can be reduced. This reduces problems, for example, in providing transparent display-pixel electrodes over the integrated diode and TFT structure.

Several basic variants are possible depending on the nature and arrangement of the etch-stop and interconnection films.

In one form, the interconnection film may comprise metal which itself provides the etch-stop film. In this case, the diode may have a vertical PIN diode structure formed in its active semiconductor film (as an intrinsic region between P and N electrode regions) deposited on the metal film.

In another form, for example, the etch-stop film may be an insulating film that extends over the interconnection film and that has a window at the diode area to permit contact between the interconnection film and the active semiconductor film of the diode. With this form, the interconnection film may be of metal. However, with this form of etch-stop film, the interconnection may even be of semiconductor material that provides a bottom one of the electrode regions of the diode (for example, a P+ or N+ doped region of a PIN diode). Thus, such a semiconductor electrode/interconnection film of the diode can be adequately protected by the insulating etch-stop film during the etch-definition of the diode layout. This permits the provision of novel device structures.

Thus, according to another aspect of the present invention, there is provided an electronic device comprising thin-film circuit elements that include a diode integrated with a crystalline thin-film TFT, wherein:

- the TFT has at least one of its source, drain and gate formed as a doped region of a crystalline semiconductor film that is more crystalline than an active semiconductor film of the diode;
- the doped region of the crystalline semiconductor film extends from the TFT to provide a bottom electrode region of the diode that is thereby interconnected with the said one of the TFT source, drain and gate; and
- the diode has its said active semiconductor film on the crystalline semiconductor film at a window in an insulating etch-stop film that extends over the crystalline semiconductor film and over at least a portion of the crystalline TFT, the active semiconductor film of the diode having a lateral extent that terminates on the insulating etch-stop film.

Various advantageous features and feature-combinations in accordance with the present invention are set out in the appended Claims. These and others are illustrated in embodiments of the invention that are now described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram of a pixel circuit of an active-matrix electroluminescent display device, illustrating an example of the context in which the present invention can be used;

Figure 2 is a cross-sectional view of parts of one pixel structure formed on a circuit substrate of such an active-matrix electroluminescent display device, in one particular embodiment of the invention;

Figures 3 to 7 are a cross-sectional view of a TFT and diode part of a pixel structure similar to that of Figure 2 at successive stages in its manufacture by a method in accordance with the invention; and

Figures 8 to 13 are cross-sectional views during manufacture, of a TFT and diode part of other pixel structures that can be manufactured by other respective methods in accordance with the invention.

It should be noted that all the Figures are diagrammatic. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features in modified and different embodiments.

FIGURE 1 EXAMPLE OF THE DISPLAY PIXEL CIRCUIT

The circuit of Figure 1 illustrates just one pixel of a pixel array of an active-matrix electroluminescent display device of the general type that is disclosed in, for example, WO-A-01/20591, WO-A-01/99190 and WO-A-01/99191. Figure 1 illustrates a particularly simple example of pixel circuit, whereas other more complex pixel circuits with more than two TFTs are also known. It will be understood that the present invention may be applied not only to the simple circuit of Figure 1, but also to these more complex pixel circuits.

As illustrated in Figure 1, each pixel comprises:

- a light-emitting element 500, typically a light-emitting diode (LED) of organic semiconductor (for example, polymer semiconductor),
- at least two polysilicon thin-film transistors (namely a drive TFT1 and an address TFT2), whereby the LED 500 is driven via the drive TFT1 as addressed via the address TFT2,
- a thin-film storage capacitor Cs for storing the drive signal applied to the gate of drive TFT1 via address TFT2, and
- an amorphous PIN photodiode D that is responsive to the light output 501 of the LED 500 and is used for regulating the operation of the LED 500 via drive TFT1 in order to counteract aging effects in the LED 500.

The present invention is illustrated in its application to the integration of a thick, vertical amorphous PIN photodiode D with drive TFT1 and/or address TFT2. As shown in Figure 1, this thin-film diode D is connected between power supply line 451 and an internal conductor line 460, in parallel with the capacitor Cs. The power supply line 451 (+Vp) is connected to the source s1 of the drive TFT1), as well as to the PIN diode D and to the capacitor Cs. The conductor line 460 is connected to both the gate g1 of drive TFT1 and the drive signal output (source s2) of the address TFT2, as well as to the PIN diode D and to the capacitor Cs. The address TFT2 has its gate g2 connected to a respective row conductor 452 of the array, and its drain d2 is connected to a respective column conductor 453 of the array. The pixel layout is such that the photodiode D receives part of the light output 501 from its respective pixel, without the pixel aperture being obscured by the capacitor Cs, TFTs TFT1 and TFT2 and their connection conductors.

Thus, the process stages used for the integration of these thin-film circuit elements D, Cs, TFT1, TFT2 on a circuit substrate 100 need to be compatible with the complex pixel context of the display device. The present invention permits integration of the amorphous PIN diode D with polysilicon transistor TFT1 and/or TFT2, in a manner that permits a good degree of optimisation of the respective properties of the diode D and TFT, while using common process

steps for their integration. Generally, the same polysilicon TFT technology and same process steps may be used to fabricate both TFT1 and TFT2 side-by-side on the circuit substrate 100, but with different TFT layouts and different connection layouts for each TFT.

Several specific embodiments for the integration of the diode D with these TFTs are now described with respect to the Figures 2 to 13. Each specific embodiment includes the stages of:

(a) forming on the circuit substrate 100 a crystalline active semiconductor film 10 for the channel areas 1 of the TFTs TFT1 and TFT2, with a first process involving a first processing temperature;

(b) forming doped source regions s1,s2 and drain regions d1,d2 of the TFTs at ends of the channel area, with a second process involving a second processing temperature;

(c) providing an interconnection film 20 between an electrode area of one of the TFTs and a diode area over which the diode D is to be formed, and providing an etch-stop film 30 on which an active semiconductor film 40 for the diode is to be deposited;

(d) thereafter depositing the active semiconductor film 40 for the diode D over the interconnection film 20 and the etch-stop film 30 with a third process that involves a third processing temperature, this stage (d) being performed after stages (a) and (b), and the first and second processing temperatures being higher than the third processing temperature; and

(e) thereafter etching away the active semiconductor film 40 for the diode D from over the etch-stop film 30 to leave the active semiconductor film 40 for the diode over the interconnection film 20 in the diode area.

Such a device manufacturing method in accordance with the invention is advantageous for providing the TFT with good quality crystalline material for its channel area and with efficient source and drain regions. This is achieved through the use of the higher first and second processing temperatures in stages (a) and (b). By carrying out stage (d) with its lower third processing temperature after stages (a) and (b), such a method is also advantageous for providing the diode D with a less crystalline material 40 (preferably even an amorphous

semiconductor material) in an appropriate film thickness for the desired diode characteristics. By depositing and etching the active semiconductor film 40 for the diode D over the etch-stop film 30 (as well as over the interconnection film 20), the layout of this semiconductor film 40 in the diode area can be defined without undesirable etching of other parts of the device such as the TFT and its interconnection to the diode D.

Such a method in accordance with the invention permits the use of one or more common films for the diode D and TFT1 and/or TFT2, depending on the nature and arrangement of, for example, the interconnection film 20 and the etch-stop film 30. Various specific embodiments will now be described.

Embodiment of Figures 2 to 7

Figure 2 illustrates the pixel structure of one embodiment of a display device as manufactured by a first embodiment of a method in accordance with the invention.

Polysilicon TFT1 and TFT2 each comprise an island of a crystalline silicon film 10 that provides each TFT with its respective channel area. Both the TFT1 island and TFT2 island are shown in Figure 2, being artificially constrained into the plane of the drawing. In a practical pixel layout, TFT1 and TFT2 would normally be in different cross sections. Both these TFTs are themselves of a known top-gate configuration which has its respective gate electrode g1,g2 on a gate dielectric film 2 on the silicon film 10 and which has its respective source s1,s2 and drain d1,d2 formed as doped regions of the film 10. In this embodiment, the source s1,s2 and drain d1,d2 of both TFTs have a p-type doping (P+), and both the TFTs are p-channel.

The address TFT2 has its gate g2 connected to row metallisation 452 of the array, and its drain d2 connected to column metallisation 453 of the array. Its source s2 is connected by internal conductor line 460 to the capacitor Cs, to the photodiode D, and (also via metallisation 461) to the gate g1 of the drive TFT1. The drive TFT1 has its drain d1 connected by metallisation 450 to the bottom transparent (ITO) electrode 561 of the pixel LED 500. As shown in Figure 2, these connections to metallisation pattern 450, 451, 452, 453, 461 (for example

of aluminium) are made via contact windows in an inter-level insulating layer 51. A further insulating layer 52 separates this metallisation pattern from the LED pixels, except at a window where the transparent display-pixel electrode 561 is connected to the TFT1 drain metallisation 450.

The present invention reduces the height of stepped increases in the topography due to the integration of the thick vertical PIN diode D. This reduces problems in providing the transparent display-pixel electrodes 561 over the integrated diode and TFT structure. The light-emitting semiconductor polymer film 560 of the pixel LED 500 is sandwiched between this electrode 561 and a grounded cathode electrode 562.

Furthermore, the present invention (as implemented in the embodiment of Figure 2) provides the interconnection film 20 in an advantageous manner for the conductor line 460, connecting the diode D and the source s2 of address TFT2. Thus, in this embodiment, a P+ doped track region of the polysilicon film 10 is used to provide this interconnection film 20 (conductor line 460).

Furthermore, a P+ region of this same film 10,20 may also provide the bottom plate of capacitor Cs. This use of the film 10,20 for the bottom plate of capacitor Cs is illustrated in the Figure 2 embodiment. In this particular example, the top plate 3 of capacitor Cs is illustrated as a separate area of the film that provides the TFT gates g1,g2. Thus, the gate dielectric film 2 may also provide the capacitor dielectric.

Thus, as illustrated in Figure 2, a continuous P+ doped track of polysilicon film 10 forms the doped source s2 of TFT2, the bottom plate of capacitor Cs, the bottom electrode region 51 of PIN diode D, and their interconnection 20. The gate g1 of TFT1 is connected to this P+ polysilicon track.

The remainder of the PIN diode D of Figure 2 is formed on this polysilicon P+ region 51 by etch-defined regions 40 and 42 of a thick amorphous intrinsic silicon film and of a thinner amorphous N+ doped silicon film. In this embodiment, the etch-stop film 30 used during the etch definition of the diode D is provided by an extension of the gate-dielectric film 2. A metal film (for example of chromium) for the top contact 45 may be present over the diode area during this etching stage, and its contact area (and obscuration) on the diode region 42

can be restricted later (for example, after defining the metallisation pattern 450, 451, 452, 453, 461).

Figure 3 illustrates stage (a) in the manufacture of this embodiment. The substrate 10 is typically of a low-cost insulating material (for example glass, or perhaps even an insulating polymer), having an insulating coating of, for example, silicon dioxide or silicon nitride providing its upper surface on which the circuit elements are formed. A silicon film 10 initially of amorphous material is deposited for the TFT islands and is crystallised in known manner by heating with a laser beam 200. Typically, an excimer laser may be used, with a laser energy and pulse rate sufficient to melt the film 10 through most of its thickness. The silicon film 10 typically reaches temperatures in the range of 1000°C to 1400°C (depending on its hydrogen content) during this laser treatment.

Figure 3 depicts three parts to this film 10, namely part [TFT] where a TFT (TFT1 or TFT2) will be formed, part [D] where the diode D will be formed, and part [20,460] where the TFT-diode interconnection will be formed. It should be noted that the Figure 3 cross-section shows the part [20,460] in link-dot outline to indicate that this part [20,460] of the film 10 is out of the plane of the drawing. This cross-section is more realistic for a display pixel layout than that of Figure 2, in which both TFT1 and TFT2, the diode D and the interconnection 20,460 were all constrained into the plan of the drawing. In the case where the part [TFT] of Figure 3 is for TFT2, the part [20,460] of the film 10 extends out of the plane of the drawing while remaining integral with the parts [TFT] and [D] which are in the plan of the drawing. In a case where the part [TFT] is for TFT1, the part [20,460] of the film 10 is not integral with this [TFT] part of Figure 3, but only with the part [D] which is in the plan of the drawing.

In order to simplify the description for the subsequent Figures 4 to 7, it will be assumed that Figure 3 shows the [TFT] part of TFT2, that the separate TFT1 island of the film 10 is also out of the plane of the drawing, and that TFT1 is fabricated with the same process steps as the depicted TFT2.

Figure 4 illustrates a subsequent stage in the manufacture, after deposition of the gate-dielectric film 2 and a film g' of metal. Typically, the film g' may be of, for example, aluminium, or chromium, or silicide or another material

or alloy commonly used for TFT gate electrodes. The gates g1 and g2 are defined from the film g' with normal photolithographic and etching techniques.

Figure 5 illustrates the later stage (b), in which the P+ regions s1,s2, d1,d2, 20(460) and 41 are formed in the polysilicon film 10. These P+ regions are formed by implanting boron ions in the film 10 (except where masked by the gates g1 and g2 and any additional mask feature) and then heating to anneal the implantation damage and activate the boron dopant. This heating step may be performed with a laser beam 201. During such laser treatment, the temperature of exposed areas of the silicon film 10 typically exceeds 900°C. Instead of a laser beam, a rapid thermal anneal (RTA) using high intensity light 201 may be used for this heat treatment. In this case, the exposed areas of the silicon film 10 typically reach a temperature in the range of 600°C to 900°C. In a further alternative, a furnace anneal in the range of 350°C to 600°C may be used. A combination of these heating treatments may even be used. Multiple implants may also be used to form differently doped regions, for example, in a LDD (low-doped drain) structure.

These stages (a) and (b) of Figures 3 and 5 with their high processing temperatures are very advantageous for the TFTs, in the achievement of good quality crystalline material for their channel area and of efficient source and drain contacts. Furthermore, by using the gate electrodes g1 and g2 as implantation masks, the P+ source and drain regions s1,s2 and d1,d2 are self-aligned with their gate electrode g1,g2.

Either before or after this doping stage (b), a window 24 is opened in the film 2 at the area where the PIN diode D is to formed. This window 24 permits contact between the interconnection film 20 (polysilicon film 2 in this embodiment) and the subsequently-deposited active diode film (amorphous intrinsic film 40 in this embodiment).

It is desirable to hydrogenate the polysilicon TFTs after depositing their gate dielectric 2 (i.e. after Figure 4). This hydrogenation stage is another treatment at a moderately high temperature, and so it is carried out before depositing the amorphous silicon material for the diode D. It may typically be a thermal anneal at 300°C to 400°C in N_2/H_2 gas (10% H_2), or it may be a

hydrogen plasma exposure at 300-400C, or a combination of both. Preferably, it should be performed after providing the gate metal and activating the dopant since any damage introduced by these two processes can then be passivated by the hydrogen. Therefore, preferably, this hydrogenation is performed after stages (a) and (b) and before stage (d), and it may be the very last process that is performed before the a-Si deposition stage (d).

Figure 6 illustrates the subsequent deposition stages for the PIN diode D, when an un-doped amorphous hydrogenated silicon film 40' is deposited for the intrinsic region 40(I) of the PIN diode D, followed by an N+ doped amorphous silicon film 42' for the N+ region 42. These amorphous films 40' and 42' are typically deposited at a temperature in the range 100°C to 300°C. By carrying out this stage (d) with its lower third processing temperature after stages (a) and (b), the photodiode D can be formed as a vertical PIN diode structure with a good quality intrinsic amorphous semiconductor region 40 in an appropriate thickness for the desired diode characteristics.

Thus, the thickness of the un-doped amorphous silicon film 40' is chosen as desired for efficient absorption of the LED output 501 by the intrinsic region 40(I) of the PIN diode D, even at the red end of the spectrum. In a typical embodiment of an active matrix electroluminescent colour display, efficient PIN photodiodes can be formed with an intrinsic amorphous silicon film that has a thickness in the range of, for example, 0.5μm to 1.0μm. This is much thicker than the polysilicon film 10 of the TFTs, which may have a thickness in the range of, for example, 0.04μm to 0.10μm.

Thereafter, the lateral dimensions of the PIN diode D are defined in the films 42' and 40' with normal photolithographic and etching techniques, but using the gate-dielectric film 2 as an etch-stop 30. Thus, this etch-stop film 2,30 prevents undesirable etching of other parts of the device, such as the polysilicon film 10 that forms the TFT islands and the interconnection 20,460 to the diode D. During this etching step, a top metal film 45' (for example of chromium) may be present over the diode area as at least part of the etchant mask. Its lateral extent can be restricted at a subsequent stage (after defining the metallisation pattern

450, 451, 452, 453, 461) to give the desired contact area (and edge-only obscuration) of the top metal contact 45 on the diode region 42.

Two unusual aspects of this embodiment are to be seen in the resulting structure of PIN diode D, namely:

- dielectric layer 2,30 is interposed between the edge of the P+ lower electrode region 41 of the PIN diode D and its intrinsic region 40, and
- the P+ lower electrode region 41 of this amorphous PIN diode is formed in the polysilicon film 10, i.e. a hybrid of technologies.

The number of process steps and mask steps is reduced by using in this way common films 10 and 2,30 in the TFT and diode and for the interconnection and etch stop. Thereafter, the manufacture of the device is continued in known manner.

In this embodiment, the TFT gates g1 and g2 were provided before the source/drain formation stage (b) so producing a self-aligned structure. However, the present invention may be used with non-self-aligned TFTs, in which the channel area of the film 10 is masked with, for example, photoresist during the dopant implant of the source/drain formation stage (b). Thereafter, the TFT gates g1 and g2 can be provided, for example with the same metallisation film as used for a top metallisation 420 of the PIN diode D. A separate part of this gate metallisation film may even form, for example, an interconnection between the top metallisation 420 of the PIN diode D and the source s1 of the drive TFT1.

Embodiment of Figure 8

In the embodiment of Figures 2 to 7 the interconnection film 20 and the bottom electrode region 41 of the diode D are formed in the polysilicon film 10 that provides TFT channel areas. Figure 8 illustrates a modified embodiment, in which a different interconnection film 20 provides doped-silicon gates g1 and g2 of the TFTs and the bottom electrode region 41 of the diode D. In this case, the gate-dielectric film 2 is not used as the etch stop film 30. This different interconnection film 20 provides the conductor line 460 connecting the diode D with the gate g1 of drive TFT1. Figure 8 shows the TFT1.

In this Figure 8 embodiment, the TFT polysilicon film 10 is formed by laser crystallisation, as in Figure 3. After depositing thereon the gate-dielectric film 2, the interconnection film 20 is deposited and patterned by photolithography and etching. Thus, in this embodiment, the film 20 provides both a gate film g' for the TFTs and the bottom electrode region 41 of the diode D. As was the case for the interconnection of Figures 3 to 7, the interconnection itself between the gate g1 of TFT1 and the bottom electrode region 41 of diode D is outside the plane of the Figure 8 drawing, which simply shows regions g1 and 41 at its ends.

In the Figure 8 embodiment, this film 20 (forming the interconnection itself, the TFT gate g1 and the diode bottom electrode region 41) may be doped P+ in the same boron doping stage (b) as is used to form the doped regions s1,s2 and d1,d2 of the TFTs. Thus, the TFTs may still be of the self-aligned type. Thereafter, the thin-film structure is covered with an insulating film 30 which is to provide the etch-stop (instead of using an extension of the gate-dielectric film 2), and the contact window 24 is etched therein at the diode area. Thereafter the manufacture is continued as in the embodiment of Figures 2 to 7.

Embodiment of Figure 9

The embodiments so far illustrated have top-gate TFTs. Figure 9 illustrates an embodiment with bottom-gate TFTs. In this embodiment (as in Figures 2 to 7), the polysilicon film 10 provides the interconnection 20,460 between the TFT2 and bottom electrode region 41 of the diode D, as well as providing the channel area of the TFTs.

The bottom gates g1 and g2 of the TFTs are formed (by film deposition, photolithography and etching) on the substrate 100, before stage (a) of the process. These gates g1 and g2 may be of metal or doped polysilicon. Then the gate-dielectric film 2 is deposited, followed by the silicon film 10.

By photolithography and etching, the film 10 is patterned into the required areas for the TFT islands, the bottom electrode region 41 of the diode D, and the desired interconnection 20,460 between regions s2 and 41. As was the case in Figures 3 to 8, the interconnection itself is outside the plane of the Figure 9

drawing, which simply shows regions s2 and 41 at its ends. The film 10 is converted to polysilicon material by laser crystallisation, as in Figure 3.

The P+ doping of the TFT regions s1,s2 and d1,d2 and the interconnection 20 and the diode region 41 is then provided by boron ion implantation and laser annealing, similar to Figure 5 (except that the gates g1 and g2 are now below the film 10). This P+ doping may be performed either before or after depositing the insulating etch-stop film 30. The contact window 24 is etched through both the film 30 and the film 2 in this embodiment, either before or after this P+ doping stage. Thereafter the manufacture is continued as in the embodiments of Figures 2 to 8.

Embodiment of Figure 10

The embodiment of Figure 10 is similar to that of Figure 9, except that a metal conductor 461 is formed at the diode area in the same processing steps as used to provide metal bottom-gates g1 and g2 of the TFTs. This metal conductor 461 may be an extension of the gate g1 of TFT1, so as to connect the interconnection 20,460 (via region 41) with the gate g1 of TFT1. In this case, a contact window 22 is opened in the gate-dielectric film 2 at the diode area before depositing the silicon film 10. The metal conductor 461 contacts through this window 22 the diode region 41 that is subsequently formed in the polysilicon film 10 as in the embodiments of Figures 5 and 9. Thereafter the manufacture is continued as in the embodiments of Figures 2 to 9.

Embodiment of Figure 11

The embodiment of Figure 11 also comprises the metal conductor 461 formed at the diode area in the same processing steps as used to provide metal bottom-gates g1 and g2 of the TFTs. However, Figure 11 shows TFT1 instead of TFT2. In this case, the metal conductor 461 may be an integral part of a different interconnection film 20 (now of metal) that provides the conductor line 460 between the bottom gates g1 of the TFT1, the bottom connection 461 to the diode D, and the bottom plate of capacitor Cs.

The further manufacturing stages may be similar to those of Figure 10, in that the bottom P+ region 41 of the PIN diode D may be formed by a region of the TFT polysilicon film 10. However, Figure 11 illustrates a further modification in which the bottom P+ region 41 of the PIN diode D is deposited after deposition of the insulating etch-stop film 30. In this case, contact window (between metal conductor 461 and diode region 41) is etched through both the insulating films 30 and 2 before depositing a P+ film 41' (for the diode region 41), the intrinsic film 40' (for the I region 40) and the N+ film 42' (for the diode region 42). In this case, the P+ region 41 may be of amorphous silicon material.

Embodiment of Figure 12

This embodiment is similar to that of Figure 11, in that the interconnection of gate g1 of the drive TFT1 with the diode P+ region 41 is via a metal film g1,20,461. However, in the Figure 11 embodiment, the TFTs are of the top-gate type. Thus, Figure 12 shows the metal gate g1 (and metal conductor 461) on the gate-dielectric film 2 that is deposited over the polysilicon active film 10 of the TFTs. Figure 12 depicts three parts to this metal film g1,20,461, namely part g1 (the gate of TFT1), part 461 where diode D will be deposited, and part 20 which represents their interconnection. This interconnection part 20 of the film is shown in link-dot outline in Figure 12 to indicate that it extends out of the plane of the drawing, while remaining integral with the parts g1 and 461 which are in the plan of the drawing.

In this embodiment, no additional etch-stop film 30 is needed when etch-defining the lateral extent of the amorphous diode regions 42,40,41. Thus, the silicon etch will stop at the surface of the metal film g1,20,461 and at the surface of the gate-dielectric 2.

Embodiment of Figure 13.

In the embodiments of Figures 11 and 12, a metal interconnection film g1,20,461 provides the gates g1 and g2 of the TFTs and the electrode connection to diode region 41. The diode D was provided beside the TFTs.

Figure 13 illustrates a modification in which the diode D can be provided on and/or as the gate g1 of TFT1. A very compact structure results.

In the Figure 13 embodiment, stages (a) and (b) are first carried out to form the doped source and drain regions in the polysilicon film 10. This doping may be done before or after depositing and patterning the metal film 20,461 for the gate electrodes g1 and g2 and any desired interconnect. Thereafter a stack of the amorphous silicon films 41', 40' and 42' is deposited over the gates g1,g2 and over the gate-dielectric film 2. These films 41', 40' and 42' have respective P+, I, and N+ conductivities for the PIN diode D. The films 41', 40' and 42' are then etched to leave the PIN diode over the channel area of the drive TFT1, i.e. on the gate g1 of TFT1. In this case, the gate dielectric film 2 and the metal film 20,461 (of g2 and any desired interconnect) serve as the etch-stop film.

In a modification of the Figure 13 embodiment, the P+ film can be deposited directly on the gate dielectric film 2 and patterned to form the gate electrodes g1 and g2 and any desired interconnect. Thereafter, an insulating film 30 may be deposited and provided with contact window 24 at the diode area over the channel area of TFT1. Thereafter the amorphous silicon films 40' and 42' of I and N+ conductivities are deposited and etched away except from over the TFT1 where the PIN diode is thereby formed. During this etch-definition, the insulating film 30 serves as the etch-stop, protecting the underlying g2 and any interconnect in the P+ film 41', as in Figure 8. However, in this modified embodiment of Figure 13, the PIN diode D itself provides gate g1 of TFT1.

OTHER EMBODIMENTS HAVING OTHER FEATURES

In the embodiments of Figures 2 to 13, the crystallised material of the active silicon film 10 has been described as being "polycrystalline". However, laser crystallisation nowadays has become such an efficient process that the resulting crystal grains can have dimensions comparable to the dimensions of a TFT island. Thus, in practice, the film 10 in any given TFT island may actually be monocrystalline material, i.e. the TFT1 and/or TFT2 may have an active film 10 of (what may be termed) single-crystal polysilicon.

In the embodiments of Figures 2 to 13, the crystalline active silicon film 10 has been described as being formed by a two-stage process, i.e. deposition of an amorphous or micro-crystalline silicon film and then laser crystallisation to the desired crystal grain size. However, it is also possible to deposit the silicon film 10 directly as polycrystalline material. Thus, for example, polysilicon material can be deposited directly in stage (a) by the thermal decomposition of silane (SiH_4) in the temperature range 580°C to 650°C. This temperature is still higher than that (for example, in the range 100°C to 300°C) used to provide the amorphous silicon active film 40' for the PIN diode D.

In the embodiments of Figures 2 to 13, the doped source and drain regions s1,s2 and d1,d2 have been formed by implanting dopant into previously un-doped regions of the active silicon film 10 of the TFT. However, it is also possible to deposit a doped extra polysilicon film for the electrode regions s1,s2,d1,d2,(41) etc, particularly for top-gate TFTs. This doped extra polysilicon film for the electrode regions s1,s2,d1,d2,(41) etc may be deposited and patterned (by photolithography and etching) either before or after the undoped active film 10. If provided before the film 10, the resulting top-gate TFT is sometimes termed a "staggered" configuration. If provided after the film 10, the resulting top-gate TFT is sometimes termed a "co-planar" configuration. In each case, the temperature (for example, in the range 580°C to 650°C) used to provide the doped film is still higher than that used to provide the amorphous silicon active film 40' for the PIN diode D.

In the embodiments of Figures 2 to 13, the PIN diode D was formed with amorphous silicon, particularly in its intrinsic region 40. The resulting diode has very suitable characteristics for photosensing visible light outputs of pixels in an active matrix colour display. However, the active diode film may be of, for example, micro-crystalline semiconductor material. This micro-crystalline diode structure can be integrated with a polysilicon TFT in accordance with the invention. Thus, the micro-crystalline film(s) of the diode can be deposited over one or more interconnection and etch-stop films with a processing temperature that is less than those earlier used for the polysilicon TFT in stages (a) and (b), after which the micro-crystalline film(s) can be etched away from over the etch-

stop film to leave the active micro-crystalline film for the diode over the interconnection film in the diode area.

In the embodiments of Figures 2 to 13, the PIN diode D was formed with its P+ film 41 as the bottom electrode region. However, inverted PIN diode structures may be used (with appropriate polarity reversals) in which the N+ film 42 is the bottom electrode region of the PIN diode. The polysilicon TFTs may be n-channel having n-type source and drain regions s1,s2 and d1,d2. In this case, for example, the bottom (N+) electrode region of the PIN diode may be formed as part of an N+ track in the polysilicon film that provides the source s2 of the n-channel TFT2 or that provides the gate g1 of the n-channel TFT1.

In some pixel circuits with two polysilicon TFTs TFT1 and TFT2, one TFT may be n-channel while the other TFT may be p-channel. in this case, the TFT2 area is masked while implanting the s1,d1 dopant of one conductivity type for TFT1, and the TFT1 area is masked while implanting the s2,d2 dopant of opposite conductivity type for TFT2. Both of these dopant implants and their anneal are carried out before depositing the less crystalline and/or amorphous material 40 for the diode D.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the design, manufacture and use of electronic devices comprising thin-film circuits and component parts thereof and which may be used instead of or in addition to features already described herein.

Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

CLAIMS

1. A method of manufacturing an electronic device comprising thin-film circuit elements that include a diode (D) integrated with a crystalline thin-film transistor (TFT), the transistor having a channel area (1) in an active semiconductor film (10) that is more crystalline than an active semiconductor film (40) of the diode, wherein the method includes:

(a) forming on a circuit substrate (100) the crystalline active semiconductor film (10) of the transistor with a first process involving a first processing temperature;

(b) forming doped source and drain regions (s1,s2, d1,d2) of the transistor at ends of the channel area (1) with a second process involving a second processing temperature;

(c) providing an interconnection film (20) between an electrode area (s2, g1) of the transistor and a diode area over which the diode (D) is to be formed, and providing an etch-stop film (30) on which the active semiconductor film (40') for the diode is to be deposited;

(d) thereafter depositing the active semiconductor film (40') for the diode over the interconnection film (20) and the etch-stop film (30) with a third process that involves a third processing temperature, this stage (d) being performed after stages (a) and (b), and the first and second processing temperatures being higher than the third processing temperature; and

(e) thereafter etching away the active semiconductor film (40') for the diode from over the etch-stop film (30) to leave the active semiconductor film (40) for the diode (D) over the interconnection film (20) in the diode area.

2. A method according to Claim 1, wherein the etch-stop film (30) is an insulating film (2, 300 that extends over the interconnection film (20) and that has a window (24) at the diode area to permit contact between the interconnection film and the active semiconductor film of the diode.

3. A method according to Claim 2, wherein the diode has its active semiconductor film (40) forming an intrinsic region between P and N electrode regions (41, 42) of a vertical PIN diode structure, and wherein the interconnection film (20) comprises a doped region (P+) that is formed in stage (b) in a semiconductor film (10) together with the doped source and drain regions (s1,s2, d1,d2) of the transistor and a bottom one (41) of the P and N electrode regions of the PIN diode.

4. A method according to Claim 3, wherein regions of the crystalline active semiconductor film (10) provided in stage (a) are doped in stage (b) to provide the source and drain regions of the transistor, the bottom one of the P and N electrode regions of the PIN diode, and the interconnection film therebetween.

5. A method according to Claim 3, wherein at least a portion of the interconnection film (20) is provided on a gate-dielectric film (2) on the crystalline active semiconductor film (10) to form a doped-semiconductor top gate electrode (g1) of the transistor which is thereby interconnected with the bottom one (41) of the P and N electrode regions of the PIN diode.

6. A method according to Claim 5, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

7. A method according to both Claim 4 and Claim 5, wherein the electronic device comprises first and second crystalline thin-film transistors (TFT1, TFT2) integrated with the PIN diode by means of the same interconnection film (20), and wherein the interconnection film (20) provides the bottom one (41) of the P and N electrode regions of the PIN diode, the top gate electrode (g1) of the first transistor, and/or the source and drain regions (s2, d2) of the second transistor.

8. A method according to Claim 1, wherein the interconnection film (20, 461) comprises metal which itself provides the etch-stop film (30), and the diode has a vertical PIN diode structure formed in its active semiconductor film as an intrinsic region between P and N electrode regions.

9. A method according to Claim 8, wherein at least a portion of the etch-stop interconnection film is provided on a gate-dielectric film (2) on the crystalline active semiconductor film to form a top gate electrode (g1) of the transistor which is thereby interconnected with a bottom one (41) of the P and N electrode regions of the PIN diode.

10. A method according to Claim 9, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

11. A method according to Claim 9 or Claim 10, wherein the electronic device comprises first and second crystalline thin-film transistors (TFT1, TFT2) integrated with the PIN diode by means of the same interconnection film (20, 461), and wherein the interconnection film connects the bottom one (41) of the P and N electrode regions of the PIN diode, the top gate electrode (g1) of the first transistor, and the source region (s2) of the second transistor.

12. A method according to Claim 7 or Claim 11, wherein the electronic device comprises an active-matrix electroluminescent display with a light-emitting diode (500, LED) in each pixel, and wherein the light-emitting diode is driven via the first transistor (TFT1) as addressed via the second transistor (TFT2).

13. A method according to any one of the preceding Claims, wherein the crystalline semiconductor film (10) is subjected to a hydrogenation process that is performed after stages (a) and (b) and before stage (d).

14. A method according to any one of the preceding Claims, wherein the crystalline semiconductor film (10) is formed in stage (a) by crystallising a deposited semiconductor film using laser heating (200) of the film.

15. A method according to any one of the preceding Claims, wherein the doped source and drain regions are formed in stage (b) by an ion implant of dopant in the crystalline semiconductor film and by annealing (201) the implanted dopant.

16. An electronic device comprising thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor, wherein:

the transistor has at least one of its source, drain and gate electrodes formed as a doped region (s2, g1) of a crystalline semiconductor film (10, 20) that is more crystalline than an active semiconductor film (40) of the diode,

the doped region (s2, g1) of the crystalline semiconductor film extends from the transistor to provide a bottom electrode region (41) of the diode that is thereby interconnected with the said one (s2, g1) of the transistor source, drain and gate electrodes, and

the diode has its said active semiconductor film (40) on the crystalline semiconductor film (10, 20) at a window in an insulating etch-stop film (2, 30) that extends over the crystalline semiconductor film and over at least a portion of the crystalline thin-film transistor, the active semiconductor film (40) of the diode having a lateral extent that terminates on the insulating etch-stop film.

17. A device according to Claim 16, wherein the diode has a vertical PIN structure having its said active semiconductor film as an amorphous intrinsic region (40) stacked between P and N electrode regions, and wherein the insulating etch-stop film (2, 30) extends between the bottom one (41) of the P and N electrode regions and the amorphous intrinsic region (40) at the lateral edge of the PIN diode.

18. A device according to Claim 16 or Claim 17, and comprising any ot the additional device features resulting from the use of any of the methods set out in any one of Claims 4 to 7 or 11 to 15.

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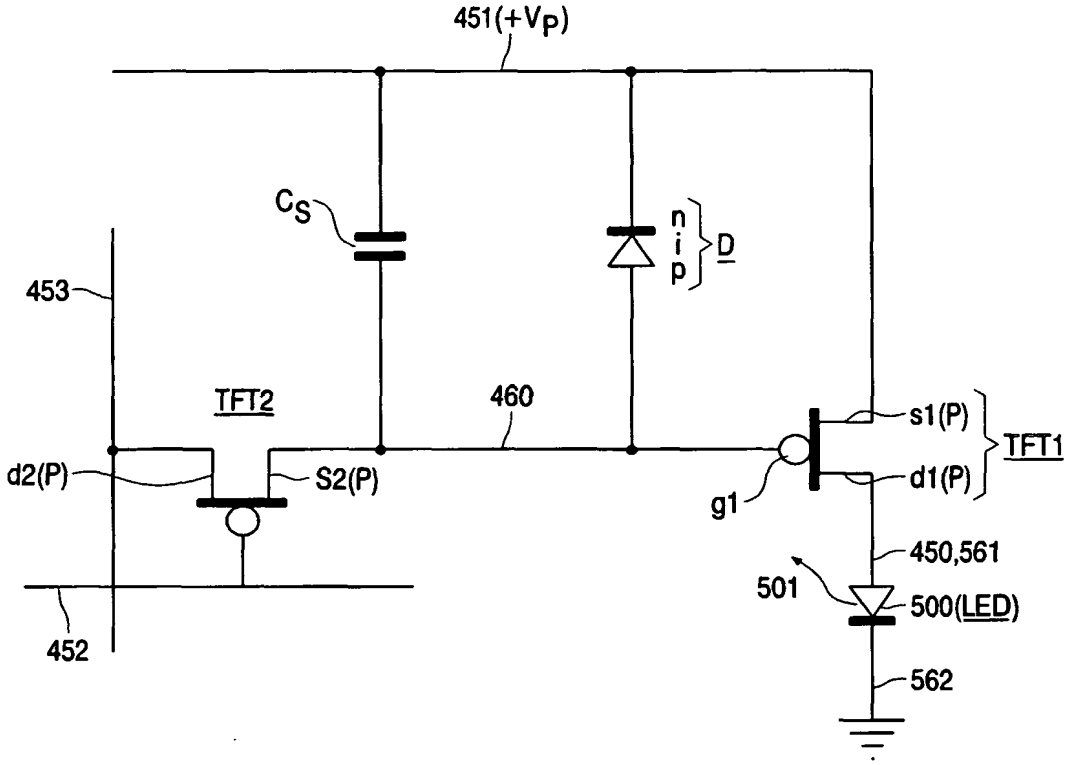
451(+VP)
CS
n
i
p
D
453
TFT2
460
s1(P)
TFT1
d2(P)
S2(P)
d1(P)
g1
450,561
501
500(LED)
452
562

FIG.1

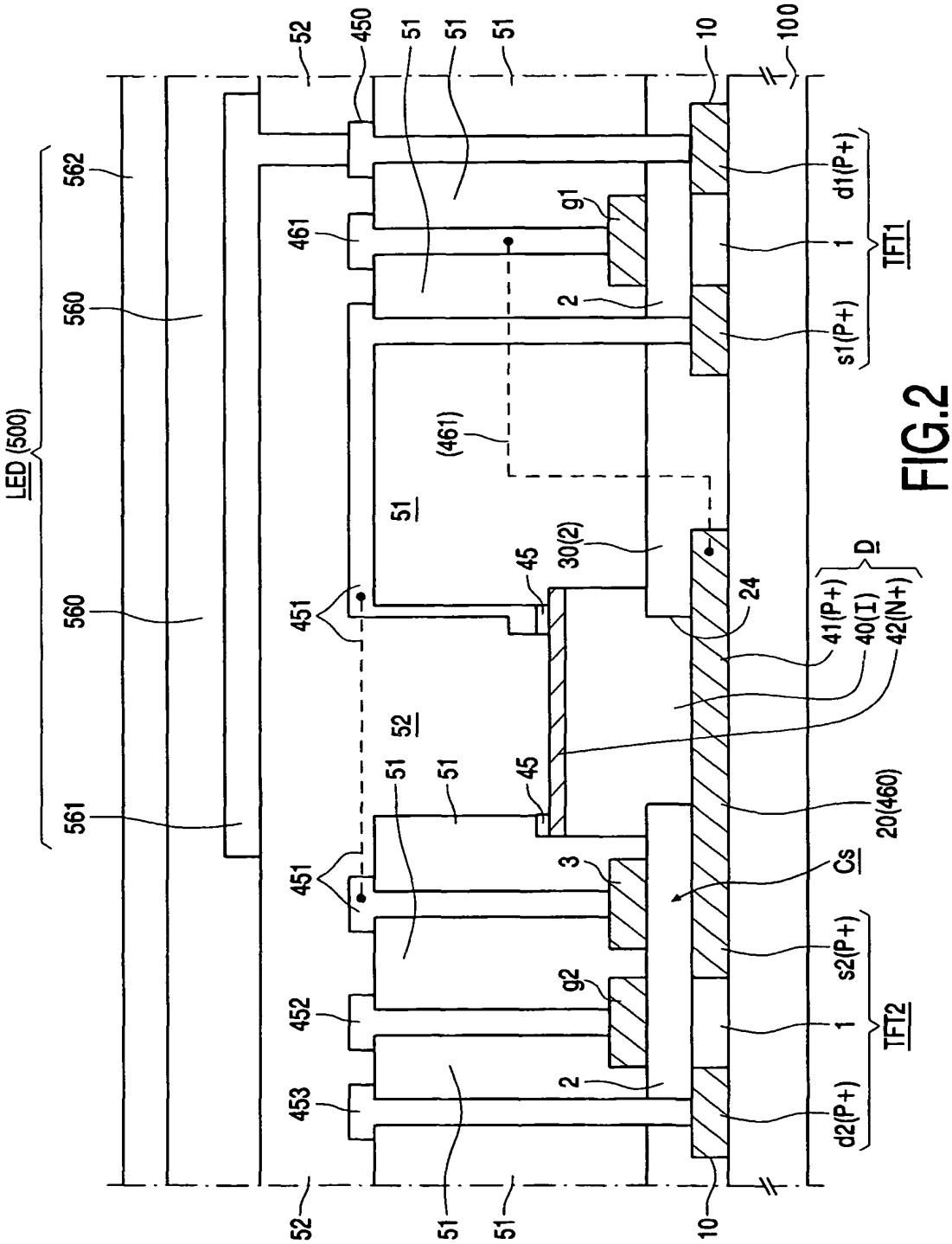
LED (500)
562
560
560
561
461
451
451
452
453
450
52
51
51
51
10
100
g1
2
(461)
51
45
30(2)
24
41(P+)
40(I)
42(N+)
D
20(460)
3
Cs
g2
d1(P+)
1
s1(P+)
TFT1
s2(P+)
1
d2(P+)
TFT2

FIG.2

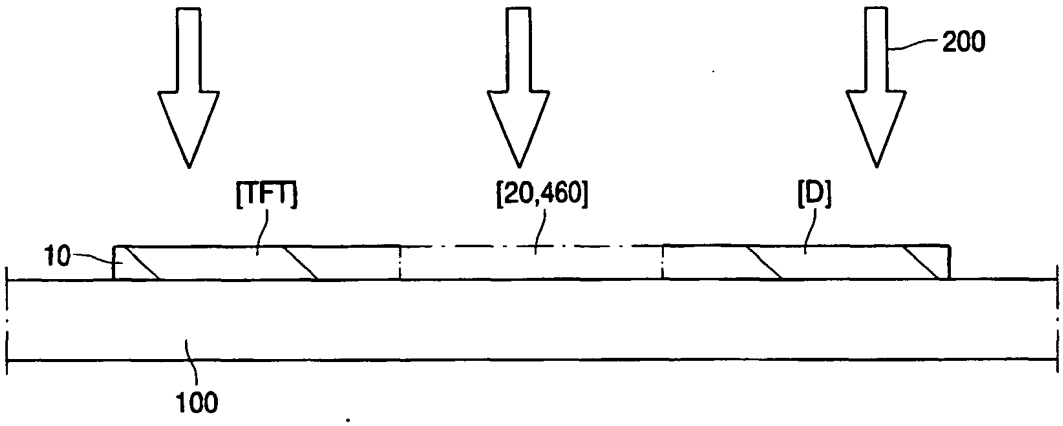

FIG.3

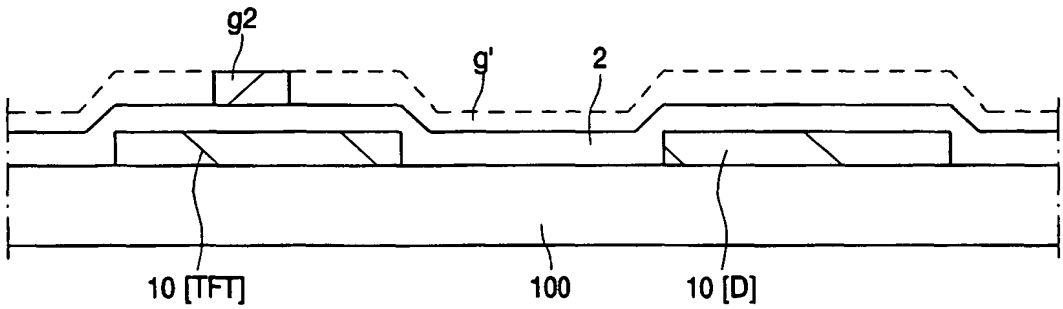

FIG.4

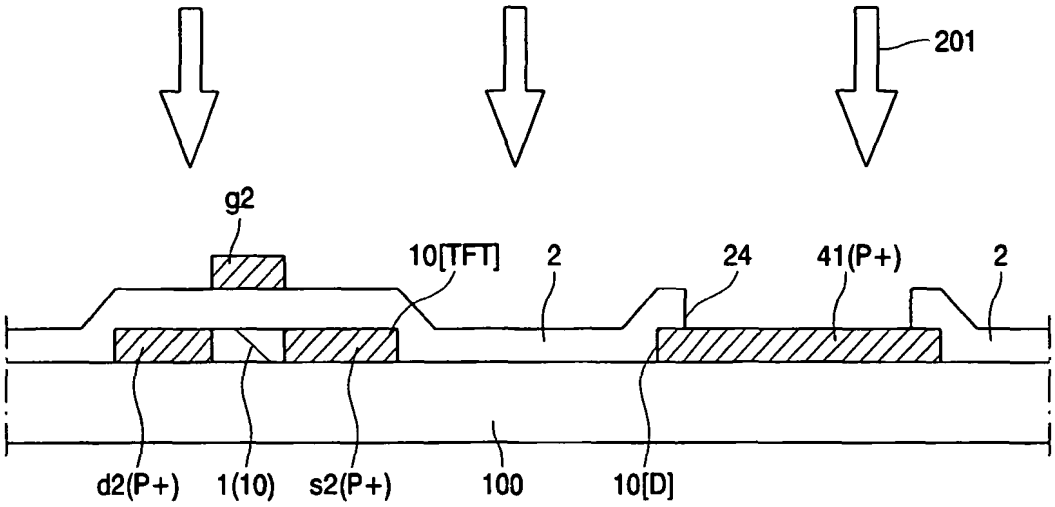
201
g2
10[TFT]
2
24
41(P+)
2
d2(P+)
1(10)
s2(P+)
100
10[D]

FIG.5

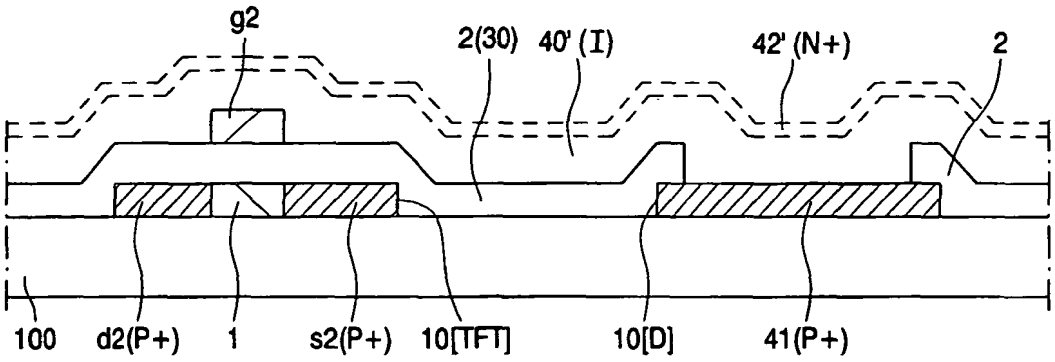
g2
2(30)
40' (I)
42' (N+)
2
100
d2(P+)
1
s2(P+)
10[TFT]
10[D]
41(P+)

FIG.6

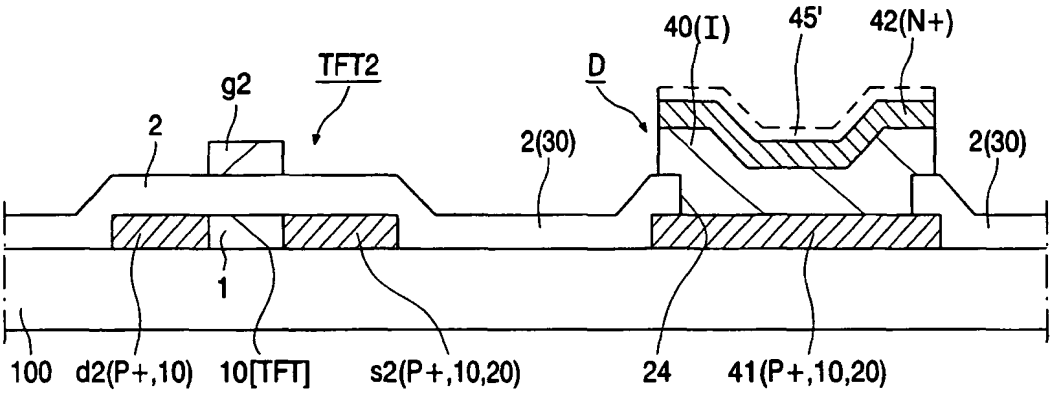
40(I)
45'
42(N+)
TFT2
g2
D
2
2(30)
2(30)
1
100
d2(P+,10)
10[TFT]
s2(P+,10,20)
24
41(P+,10,20)

FIG.7

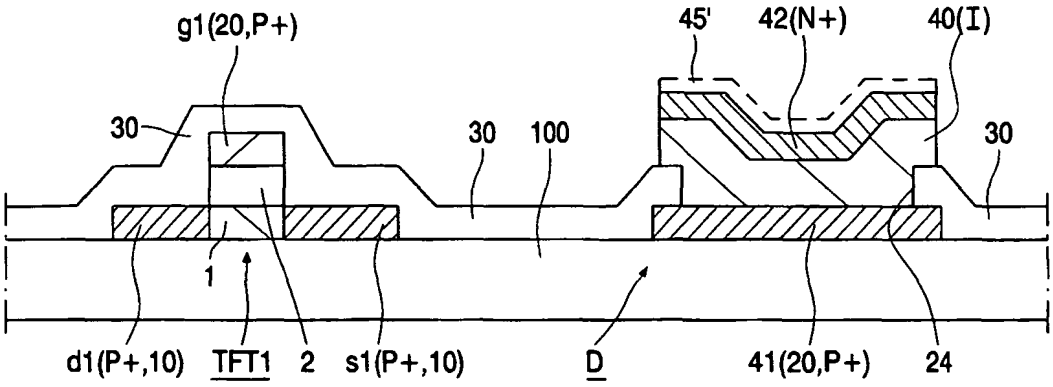
g1(20,P+)
45'
42(N+)
40(I)
30
30
100
30
1
d1(P+,10)
TFT1
2
s1(P+,10)
D
41(20,P+)
24

FIG.8

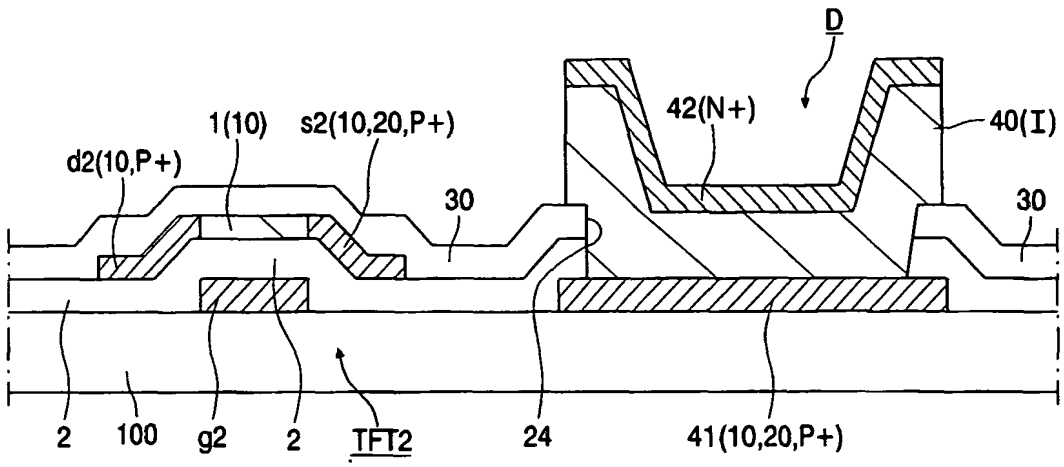

FIG.9

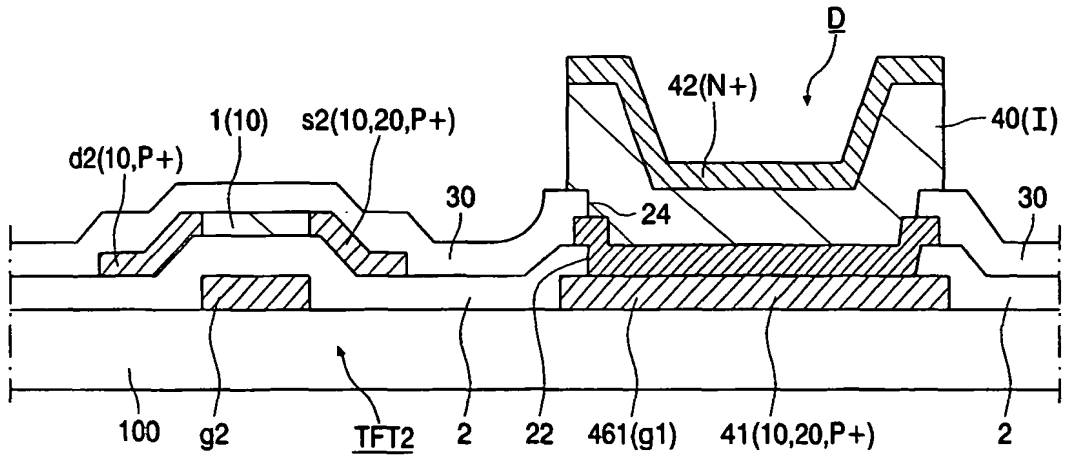

FIG.10

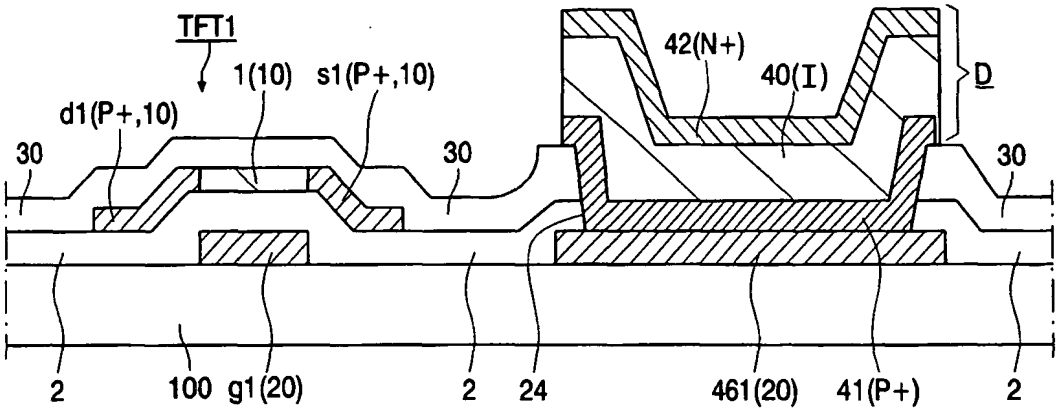

FIG.11

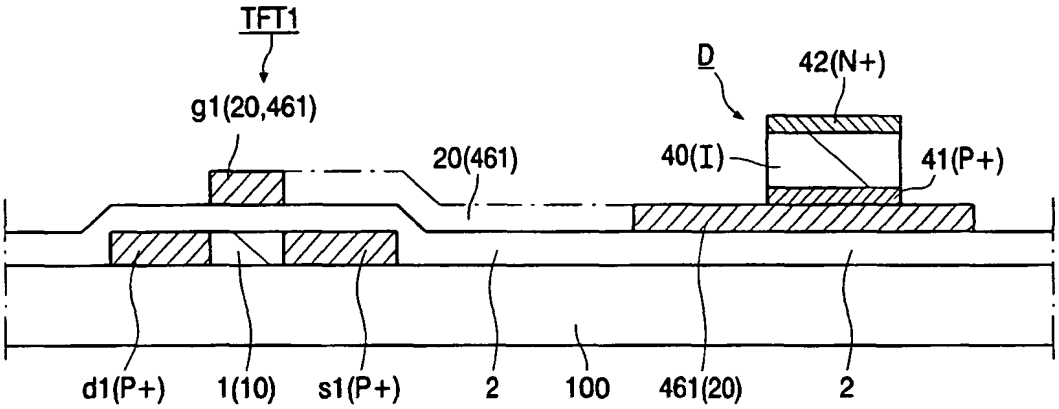

FIG.12

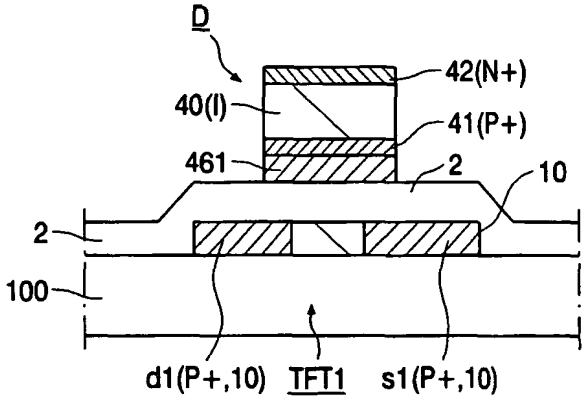

FIG.13

INTERNATIONAL SEARCH REPORT

PCT/IB 03/03484

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02F1/1362 H01L27/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 930 607 A (SATOU TAKASHI) 27 July 1999 (1999-07-27) column 10, line 23 -column 15, line 36; figures 1-26 ---	1-18
A	EP 0 909 972 A (KOPIN CORP) 21 April 1999 (1999-04-21) the whole document ---	1-18
P,A	US 2003/063429 A1 (WATANABE YOSHIHIRO) 3 April 2003 (2003-04-03) the whole document ---	1-18
P,A	US 2002/191140 A1 (FUJIKAWA SHINSUKE ET AL) 19 December 2002 (2002-12-19) the whole document -----	1-18

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 December 2003	29/12/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Boero, M

INTERNATIONAL SEARCH REPORT

PCT/IB 03/03484

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5930607 A	27-07-1999	CN 1388404 A	01-01-2003
		CN 1165568 A	19-11-1997
		WO 9713177 A1	10-04-1997
		JP 3261699 B2	04-03-2002
		KR 270468 B1	01-11-2000
		TW 438991 B	07-06-2001
		US 2003207506 A1	06-11-2003
		US RE38292 E1	28-10-2003
EP 0909972 A	21-04-1999	US 5376561 A	27-12-1994
		US 5331149 A	19-07-1994
		EP 0909972 A2	21-04-1999
		AT 180578 T	15-06-1999
		CA 2130672 A1	14-09-1993
		DE 69325110 D1	01-07-1999
		DE 69325110 T2	09-12-1999
		DK 725939 T3	15-11-1999
		EP 0725939 A1	14-08-1996
		JP 7504764 T	25-05-1995
		WO 9318428 A2	16-09-1993
		US 6140980 A	31-10-2000
		US 5583335 A	10-12-1996
		US 6636185 B1	21-10-2003
		AT 227887 T	15-11-2002
		CA 2129123 A1	19-08-1993
		DE 69332482 D1	19-12-2002
		DE 69332482 T2	02-10-2003
		EP 1237191 A2	04-09-2002
		EP 0626099 A1	30-11-1994
		JP 7504782 T	25-05-1995
		US 6486929 B1	26-11-2002
		WO 9316491 A1	19-08-1993
		US 5377031 A	27-12-1994
		US 6143582 A	07-11-2000
		US 5702963 A	30-12-1997
		US 5499124 A	12-03-1996
		US 2001040644 A1	15-11-2001
		US 5757445 A	26-05-1998
		US 6521940 B1	18-02-2003
		US 5256562 A	26-10-1993
		US 6424020 B1	23-07-2002
		US 6043800 A	28-03-2000
		US 6072445 A	06-06-2000
US 2003063429 A1	03-04-2003	JP 2003163276 A	06-06-2003
		JP 2003163277 A	06-06-2003
		CN 1405805 A	26-03-2003
		JP 2003163223 A	06-06-2003
US 2002191140 A1	19-12-2002	JP 2003066113 A	05-03-2003
		CN 1391132 A	15-01-2003